An Ultra-stable Event Timer

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**Characteristics**

- Resolution: 1 ps
- Dynamic: 64 bits
- External Clock Frequency: 10 or 100 MHz
- Precision < 3 ps
- Linearity: 1 ps rms ( +/- 1.5 ps)
- Dead time: 10 μs
- 2 independent channels
- 2 inputs per channel
Characteristics

- Automatic internal calibration
- Internal memory: 10,000 measurements
- Interface: RS 422 @ 1 MBits
- Size: 19 inches rack 3U x 280 mm
OCA Event timer synoptic
2 vernier cards

- Frequency: 50 MHz
- Resolution: 1 ps
- Dead time: 10 µs
Frequency Synthesis card

- Ultra low noise local oscillator @ 100 MHz
  - Phase noise: 100 Hz : -130 dBc, 10 kHz : -165 dBc
- Digital phase lock loop: 20 bits
- Input frequency: 10 MHz
- Output frequency: 100 MHz and 10 MHz
- Thermal sensitivity < 100 fs/°C (10 to 30 °C)
- Calibration events
3 programmable cards

- Digital timer: 10 ns resolution
- Frequency synthesis control (20 bits)
- Global control
  » Memory (10 000 events)
  » 16 bits Analog to digital converter
  » RS 422 serial interface
OCA Event Timer
Ground design
OCA Event Timer
Preliminary Space Design (EREMS)

- Mass: 7 kg
- Size: 250×240×130 mm³
- Power: 40 W
Asynchronous Test Bench
Thales Event timers

- 2 event timers (5 & 2 ps rms)
- 200 MHz frequency synthesis
- Global control
  - Memory (10 000 events)
  - 16 bits Analog to digital converter
  - RS 422 serial interface
Spectral density of the vernier linearity error

Linearity: 1 ps rms, +/- 1.5 ps
Synchronous Test Bench

[Diagram showing a synchronous test bench with labeled components such as Clock, Thales Frequency Synthesis, Flip flop, OCA Event Timer, and % 10000, with connections indicating clock frequencies of 10 MHz, 200 MHz, and 1 kHz.]
Time stability
Thermal sensitivity
Vernier linearity

Linearity: 1 ps rms, +/- 1.5 ps